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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/837,887	04/18/2001	Ram Voorakaranam	P 6079.11005	8350

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EXAMINER	
WACHSMAN, HAL D	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/837,887	VOORAKARANAM ET AL.	
	Examiner	Art Unit	
	Hal D Wachsman	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4-24-02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The drawings are objected to because they are informal drawings. Formal drawings are required and per 37 C.F.R. 1.121 each of the formal drawing sheets which the Applicant submits to replace the informal drawings must be identified in the top margin as "Replacement Sheet".

2. The declaration is objected to because there is a cross-out on the date of signature for inventor Sasikumar Cherubal as well as a cross-out on the date of signature for inventor Alfred V. Gomes both of which were not initialed and dated. In addition, the application claims the benefit under 35 U.S.C. 119(e) of provisional applications 60/197,749 and 60/203,602. However, 60/197,749 has a different title of "ATPG For Prediction of Analog Specifications" as well as a different inventive entity and is an expired provisional application. Provisional application 60/203,602 is also an expired provisional application with a different title too of "Test Generation for High Frequency and RF Circuits" as well as a different inventive entity. In addition, the parent case 09/575,488 did not have priority to either of the two above cited provisional applications but rather had priority under 35 U.S.C. 119(e) of provisional application 60/134,800. Because of the above, it is not clear exactly the basis for the claim of benefit under 35 U.S.C. 119(e) to provisional applications 60/197,749 and 60/203,602. Appropriate explanation/correction is required.

3. The statement of continuing data on page 1 of the specification is objected to because of the claim of benefit to provisional applications 60/197,749 and 60/203,602 for reasons already stated in paragraph 2 above and because the current status of U.S.

application serial no. 09/575,488 has not been provided. Appropriate correction is required.

4. Appendix A referred to on page 4 of the specification is an improper Appendix because appendices are limited to computer program listings (see 37 C.F.R. 1.96). In addition, the Examiner respectfully notes that this appendix has a different inventive entity than the instant application. Appropriate correction is required.

5. The attempt to incorporate subject matter into this application by reference to "Test Generation for Accurate Prediction of Analog Specifications" and"Low-Cost Signature Testing of RF Circuits" (see page 4 of the specification)are improper because essential material may not be incorporated by reference to non-patent publications. Appropriate correction is required.

6. The Brief Description of the Drawings on page 4 of the specification refers to Figure 6 as a flow chart however Figure 6 is an apparatus diagram. Appropriate correction is required.

7. The Examiner respectfully notes that on page 6, line 8, it appears that a right parentheses is missing.

8. On the IDS 1449 form filed 4-24-02 the cited Balivada et al. reference was not considered because the prior art reference was not in the prior art of the image file wrapper. A different Balivada et al. reference though was found in the submitted prior art and that has been considered on the attached PTO 892 form.

9. Claim 9 is objected to under 37 C.F.R. 1.75(i) because each element of the claim is not separated by a line indentation. Appropriate correction is required.

10. Claims 1-17 are objected to under 37 C.F.R. 1.75(a) for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The preamble of claim 1 cites "A method for low cost signature testing..." however the body of the claim does not make a clear reference to low cost signature testing. Claim 1, line 4, cites "said performance parameters" however the antecedent basis is "selected set of performance parameters". This same type of problem occurs in various other locations throughout the claims. Claim 1, line 12, cites "measuring said performance parameters independently of said model" however independently in what way exactly ? Claim 1, line 14, cites "said test stimulus" however the antecedent basis is "selected test stimulus". This same type of problem occurs at other various locations in the claims. Claim 4, line 3, cites "the optimized said test stimulus" which it appears should be "the optimized test stimulus". This same type of problem also occurs in claim 5, lines 1-2, claim 7, line 2, claim 12, line 3, claim 13, line 2, claim 15, line 2. Claim 5, line 2, cites "said manufactured circuit" however the antecedent basis is "manufactured electronic circuit". This same type of problem also occurs in various other locations of the claims. Claim 5, line 5, cites "said model" however is this referring to the non-linear model. Claim 6, line 2, cites "said training circuits" however the antecedent basis is "one or more manufactured training circuits". This same type of problem also occurs in various other locations in the claims. Claim 6, line 5, cites "said threshold" however the antecedent basis is "predetermined threshold". This same type of problem also occurs in claim 14, line 6. Claim 7, line 5, cites "said output" however is this referring to the signature output ? In claim 8, line 2, "RF" should be defined. This same type of problem

also occurs in claim 16, line 2. Claim 9, line 3, cites "a computerized model" however computerized in what way exactly ? This same type of problem also occurs in claim 12, line 1. Claim 9, line 8, cites "computer program adapted to command..." however if there are no instructions here on a computer readable medium that are being executed there is ambiguity with respect to how the functionality of this computer program is being realized. Claim 9, line 10, cites "corresponding measured values" however measured values by what ? Claim 17, line 2, cites "said output" however exactly which output is being referred to here ? The examiner asks the applicant to better claim the limitations cited above. While the examiner understands the intentions of the applicant he feels confusion could be drawn from the limitations cited above. Appropriate correction is required.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1-7 and 9-15 are rejected under 35 U.S.C. 102(a) or 102(b) as being anticipated by "Test Generation for Accurate Prediction of Analog Specifications" (Voorakaranam et al.).

As per claim 1, Voorakaranam et al. (section 1.0 Background, section 2.0 Overview of the proposed approach) disclose "constructing a model for predicting said performance parameters for a first electronic circuit...receiving the output of one or more second electronic circuits produced by the manufacturing process and stimulated with a selected test stimulus". Voorakaranam et al. (section 2.0 Overview of the proposed approach) disclose "providing said output to said model". Voorakaranam et al. (section 2.0 Overview of the proposed approach) disclose "obtaining a prediction of said performance parameters by use of said model". Voorakaranam et al. (section 2.0 Overview of the proposed approach) disclose "measuring said performance parameters independently of said model". Voorakaranam et al. (section 2.0 Overview of the proposed approach, section 3.0 Test generation for accurate specification prediction, section 4.0 Experimental results) disclose "iteratively varying said test stimulus to minimize the error between said prediction and the corresponding measured values...for determining an optimized test stimulus".

As per claim 2, Voorakaranam et al. (see at least abstract) disclose the feature of this claim.

As per claim 3, Voorakaranam et al. (section 2.0 Overview of the proposed approach, section 3.0 Test generation for accurate specification prediction) disclose the feature of this claim.

As per claim 4, Voorakaranam et al. (section 2.0 Overview of the proposed approach) disclose the feature of this claim.

As per claim 5, Voorakaranam et al. (section 2.0 Overview of the proposed approach, section 3.1 Specification Prediction) disclose the feature of this claim.

As per claim 6, Voorakaranam et al. (section 2.0 Overview of the proposed approach, section 3.0 Test generation for accurate specification prediction) disclose the feature of this claim.

As per claim 7, Voorakaranam et al. (section 2.0 Overview of the proposed approach, section 3.0 Test generation for accurate specification prediction) disclose the feature of this claim.

As per claim 9, Voorakaranam et al. (Abstract, section 1.0 Background, section 2.0 Overview of the proposed approach) disclose "a computerized model for predicting said performance parameters for a first electronic circuit...receiving the output of one or more second electronic circuits produced by the manufacturing process and stimulated with a selected test stimulus". Voorakaranam et al. (Abstract, section 2.0 Overview of the proposed approach, section 3.0 Test generation for accurate specification prediction, section 4.0 Experimental results) disclose " a device for iteratively varying said test stimulus, and a computer program adapted to command said device to iteratively vary said test stimulus so as to minimize the error ...corresponding measured values for said performance parameters, for determining an optimized test stimulus".

As per claim 10, Voorakaranam et al. (see at least abstract) disclose the feature of this claim.

As per claim 11, Voorakaranam et al. (section 2.0 Overview of the proposed approach, section 3.0 Test generation for accurate specification prediction) disclose the feature of this claim.

As per claim 12, Voorakaranam et al. (section 2.0 Overview of the proposed approach) disclose the feature of this claim.

As per claim 13, Voorakaranam et al. (section 2.0 Overview of the proposed approach, section 3.1 Specification Prediction) disclose the feature of this claim.

As per claim 14, Voorakaranam et al. (section 2.0 Overview of the proposed approach, section 3.0 Test generation for accurate specification prediction) disclose the feature of this claim.

As per claim 15, Voorakaranam et al. (section 2.0 Overview of the proposed approach, section 3.0 Test generation for accurate specification prediction) disclose the feature of this claim.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claims 8, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Test Generation for Accurate Prediction of Analog Specifications" (Voorakaranam et al.) in view of "Low-Cost Signature Testing of RF Circuits" (Voorakaranam et al.).

As per claim 8, "Low-Cost Signature Testing of RF Circuits" (Abstract, section 1.0 Introduction, section 2.0 Proposed Approach, section 3.0 Experimental results) teach the feature of this claim. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the techniques of "Low-Cost Signature Testing of RF Circuits" to the invention "Test Generation for Accurate Prediction of Analog Specifications" as specified above because as taught by "Low-Cost Signature Testing of RF Circuits" (section 1.0 Introduction page 3) it would provide a highly cost-effective solution for production testing of RF circuits.

As per claim 16, "Low-Cost Signature Testing of RF Circuits" (Abstract, section 1.0 Introduction, section 2.0 Proposed Approach, section 3.0 Experimental results) teach the feature of this claim. It would have been obvious to a person of

ordinary skill in the art at the time the invention was made to apply the techniques of "Low-Cost Signature Testing of RF Circuits" to the invention "Test Generation for Accurate Prediction of Analog Specifications" as specified above because as taught by "Low-Cost Signature Testing of RF Circuits" (section 1.0 Introduction page 3) it would provide a highly cost-effective solution for production testing of RF circuits.

As per claim 17, "Low-Cost Signature Testing of RF Circuits" (section 1.0 Introduction, section 2.0 Proposed Approach, section 3.0 Experimental results) teach the feature of this claim. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the techniques of "Low-Cost Signature Testing of RF Circuits" to the invention "Test Generation for Accurate Prediction of Analog Specifications" as specified above because as taught by "Low-Cost Signature Testing of RF Circuits" (section 1.0 Introduction page 3) it would provide a highly cost-effective solution for production testing of RF circuits.

15. The following references are cited as being art of general interest: Dahbura et al. (4,991,176) which disclose the generation of test sequences according to minimum cost function, Niwa et al. (5,341,315) which disclose a test pattern generation device and Chatterjee et al. (6,625,785) which disclose optimized tests in testing analog circuits.

16. No claims are allowed.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hal D Wachsman whose telephone number is 571-272-2225. The examiner can normally be reached on Monday to Friday 7:00 A.M. to 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on 571-272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hal D. Wachsman
Hal D Wachsman
Primary Examiner
Art Unit 2857

HW
September 16, 2004